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SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device, particularly to a technique of improving withstanding operating voltage.

10 2. Description of the Related Art

Fig. 5 is a sectional view describing a conventional semiconductor device.

15 In Fig. 5, symbol 51 refers to a first conductive P type semiconductor substrate. On the substrate 51, a gate electrode 53 is formed through a gate oxide film 52, and a source-drain region of a one-sided LDD (Lightly Doped Drain) structure is formed adjacent to the gate electrode 53. That is, this semiconductor device has a source-drain region of the one-sided LDD structure. A high concentration (N+ type) source region 55
20 is formed at the source region side adjacent to the gate electrode 53, a low concentration (N- type) drain region 54 is formed at the drain region side adjacent to said gate electrode 53, and a high concentration (N+ type) drain region 56 is formed in the

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low concentration drain region 54.

As described above, in the semiconductor device of the one-sided LDD structure in which a high voltage is applied only to the drain region side, the high concentration drain region 56 is surrounded by the low concentration drain region 54 to defuse concentration of electric field in the drain region side, as mentioned above. However, in the source region side, only the high concentration source region 55 exists.

Even the semiconductor device having such a structure is needless to take its structure as a particular problem with regard to static withstanding voltage. However, at operation, the following problem occurs.

That is, in a bipolar structure consisting of a source region (emitter region), a substrate (base region), and a drain region (collector region), injection efficiency of carrier is good because a high concentration source region 55 is exposed in emitter region, so that the bipolar structure can be made easily by a little substrate current I_{sub} .

That is, since current gain β in the bipolar structure with a one-sided LDD structure is high, the drain withstanding voltage during operation decreases compared with a semiconductor device of a double-sided LDD structure.

Here, in order to improve the drain withstanding voltage

during operation, the substrate current I_{sub} needs to be decreased. That is, the electric field must be made weak.

However, when an impurity concentration of the entire low concentration drain region 54 is decreased in order to decrease the substrate current I_{sub} , the substrate current I_{sub} has a double hump structure having two peaks ((1) and (2)) as voltage V_g increases, as shown in Fig. 6.

When the low concentration drain region 54 is further decreased, the first peak (1) of the substrate current I_{sub} is low so that the drain withstanding voltage at low V_{gs} improves. However, the second peak (2) of the substrate current I_{sub} is comparatively high so that drain withstanding voltage at high V_{gs} decreases.

Conversely, when the entire impurity concentration of the low concentration drain region 54 is high, a single peak at a certain voltage V_{gs} appears and the drain withstanding voltage at high V_{gs} decreases, as shown in Fig. 6. However, there is a problem that the drain withstanding voltage at low V_{gs} can not withstand.

Thus, when the entire impurity concentration of the low concentration drain region 54 is changed uniformly, the change can not overcome the trade-off relationship of the drain withstanding voltage at low V_{gs} and the drain withstanding voltage

at high V_{gs} .

Although current gain β decreases and the withstanding voltage withstands decidedly by adopting a double-sided LDD structure, the device has distance (L) of a drift region similar to the drain side shown in Fig. 5. In this instance, the on-resistance increases and the driving ability decreases because a usual LDD structure is adopted at the source side, although the withstanding voltage at the source side is not needed.

SUMMARY OF THE INVENTION

The invention is a semiconductor device comprising: a gate electrode formed on a first conductive type semiconductor substrate via a gate oxide film; a first low concentration drain region of a second conductive type, being formed adjacent to one end of the gate electrode; a second low concentration drain region of the second conductive type, being formed in the first low concentration drain region so that the second low concentration drain region is very close to the outer boundary of the first low concentration drain region, and being higher in impurity concentration than at least impurity concentration of the first low concentration drain region; and a high concentration source region of the second conductive type being formed adjacent to another end of the gate electrode and a high concentration drain

region of the second conductive type being formed in the low concentration drain region having a predetermined distance from the one end of the gate electrode.

A method for manufacturing a semiconductor device comprises:

- 5 a first process comprising steps of a first step forming a first photo resist film having a first opening at a drain forming region on a first conductive type semiconductor substrate, a second step ion-implanting a first impurity of the second conductive type and a second impurity of the second conductive type with
- 10 the first photo resist film being used as a mask, and a third step forming a first low concentration drain region of the second conductive type and a second low concentration drain region of second type by diffusing the first impurity and the second impurity after the fore-mentioned ion-implanting step; a second process
- 15 forming an element separation film at a predetermined region by selectively oxidizing with an oxidization resist film formed on the substrate as a mask and forming a second gate oxide film at region except the element separation film and the first gate oxide film; a third process forming a gate electrode so as to
- 20 cover from the first gate oxide film to the second gate oxide film; a fourth process forming a second photo resist film having a second opening on the source forming region on the substrate and having a third opening on a region separated from another

end of the gate electrode on the low concentration drain region;
and a fifth process forming high concentration source-drain regions
of the second conductive type by ion-implanting a third impurity
of the second conductive type on the substrate with the second
5 photo resist film, the gate electrode, the element separation
film, and the first gate oxide film as a mask.

Thus, the second low concentration drain region higher in
impurity concentration than impurity of the first low concentration
drain region is formed in the first low concentration drain region
10 of second conductive type so that the second low concentration
drain region is very close to the outer boundary of the first
low concentration drain region. By that, the low concentration
drain region is made with a double structure consisting of two
kinds of impurity ions different in diffusion coefficient without
15 uniformly changing impurity distribution in the low concentration
drain region. Therefore, the first low concentration drain region
withstands low V_{gs} withstanding voltage, and the second low
concentration drain region withstands high V_{gs} withstanding
voltage.

20 Further, the process forming the first low concentration
drain region and second low concentration drain region have a
process thermal-treating, at the same time, the first impurity
consisting of phosphorus ion and the second impurity consisting

of arsenic ion and use difference of diffusion coefficients of these impurities.

Thus, since difference of diffusion coefficients of two kinds of impurities is used and these impurities are formed at the same process when the first low concentration drain region and the second low concentration drain region are formed, the second low concentration drain region can be formed accurately at very near part in the first low concentration drain region.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a method for manufacturing a semiconductor device according to an embodiment of the invention. Fig. 2 is a sectional view showing a method for manufacturing a semiconductor device according to an embodiment of the invention.

Fig. 3 is a sectional view showing a method for manufacturing a semiconductor device according to an embodiment of the invention.

Fig. 4 is a sectional view showing a method for manufacturing a semiconductor device according to an embodiment of the invention.

Fig. 5 is a sectional view showing a conventional semiconductor device.

Fig. 6 graphically shows a problem in connection with the device shown in Fig. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a semiconductor device of the present invention and a method for manufacturing the semiconductor device according to the present invention will be described referring to figures.

In a semiconductor device according to the invention, a gate electrode 9 is formed on a P type substrate, for example, a semiconductor substrate 1 and disposed over from a first gate oxide film 7A to a second gate oxide film 8, as shown in Fig. 4.

A high concentration (N+ type) source region 10 is formed adjacent to one end of the gate electrode 9 (one end of the second gate oxide film 8). Further, a first low concentration (LN type) drain region 5 is formed adjacent to the other end of the gate electrode 9 (the other end of the first gate oxide film 7A). A second low concentration (SLN type) drain region 6 at least higher in impurity concentration than the first low concentration (LN type) drain region 5 is formed in the first low concentration (LN type) drain region 5 so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5. Further in the drain region 6, a high concentration (N+ type) drain region 11 is formed at

a region separated from the gate electrode 9 (so as to be adjacent to one end of the first gate oxide film 7A).

Thus, the second low concentration (SLN type) drain region 6 higher in impurity concentration than the first low concentration (LN type) drain region 5 is formed in the first low concentration (LN type) drain region so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5. By that, a low concentration drain region is made with a double structure consisting of two kinds of impurity ions differing in diffusion coefficient. That is, the drain region has the second low concentration (SLN type) drain region 6 thinly covering the first low concentration (LN type) drain region 5, without changing uniformly the impurity distribution in the low concentration drain region. Therefore, the first low concentration (LN type) drain region 5 withstands a low V_{gs} withstanding voltage, and the second low concentration (SLN type) drain region 6 withstands a high V_{gs} withstanding voltage to improve the drain withstanding voltage during operation.

Thus, by the construction of the low concentration drain region with two or more kinds of different impurity concentrations, and by not changing the impurity distribution uniformly over the entire low concentration drain regions, the drain withstanding voltage during operation can be improved independent of the

trade-off relationship of drain withstanding voltage at low V_{gs} and the drain withstanding voltage at high V_{gs} .

Because there is no need to adopt the conventional semiconductor device of the LDD structure having substantially symmetrical low concentration source-drain regions in the source-drain regions and because the device according to the present invention does not have a drift region compared with the conventional semiconductor device, the driving ability is not suppressed.

A method for manufacturing the above-mentioned semiconductor device will be described below referring to the figures.

First, in Fig. 1, a photo resist (PR) film 2 having an opening on a drain forming region on a P type semiconductor substrate 1 is formed, while using the photo resist (PR) film 2 as a mask.

First and second impurity implantation regions are formed by ion-implanting first and second impurities. The second impurity is required to have a diffusion coefficient less than the first impurity. If the first impurity is phosphorus-ion, the second impurity can be arsenic-ion, for example. After a first impurity implantation region 3 is formed by ion-implanting phosphorus-ions with an acceleration voltage of 100 KeV at a dose of about $6 \times 10^{12}/\text{cm}^2$, a second impurity region 4 is formed by ion-implanting arsenic-ions with an acceleration voltage of 160 KeV at a dose

of about $5 \times 10^{11}/\text{cm}^2$.

Next, in Fig. 2, after removing the photo resist film 2, a first low concentration (LN type) drain region 5 is formed by thermally diffusing the phosphorus ions and arsenic ions.

5 A second low concentration (SLN) drain region 6 with higher impurity concentration than at least the low concentration drain region 5 is formed in the low concentration drain region so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5.
10 At this time, a thermal treatment of about 1100°C and 4 hours is carried out.

In the process, two kinds of impurity ions (phosphorus and arsenic) having different diffusion coefficients are ion-implanted using the same mask (photo resist film 2) and diffused
15 using the difference in diffusion coefficients. Thus, the second low concentration (SLN type) drain region 6 with comparatively high impurity concentration can be formed with the thin first low concentration (LN type) drain region 5 suitably spaced apart.

Next, in Fig. 3, after forming a pad oxide film and a silicon
20 nitride film as an oxidation resistance film having an opening at the designated region (a first gate oxide film forming region and an element separation film forming region) not shown on the substrate 1, a first gate oxide film 7A and an element separation

film 7B of about 1000 nm thickness are formed by using the silicon nitride film as a mask and oxidizing the oxidation resistance film selectively by a known LOCOS method. Further, after removing the pad oxide film and silicon nitride film, a second gate oxide
5 film 8 of 150 nm thickness is formed by thermal-oxidizing the substrate where the first gate oxide film 7A and element separation film 7B are not formed. Then, after a polysilicon film of 400 nm thickness is formed on the substrate 1 and a conducting treatment of the polysilicon film is carried out, a gate electrode 9 is
10 formed to dispose over from the first gate oxide film 7A to the second gate oxide film 8, patterning a photo resist film, not shown, which is used as a mask. At this time, the second gate oxide film 8 on the substrate 1 except the part where the gate electrode 9 is formed is removed.

15 Further, in Fig. 4, an N type impurity is ion-implanted to be adjacent to one end of the gate electrode 9 using a photo resist (PR) film 12 formed on the substrate 1 as a mask. An ion-implanting N type impurity is also deposited at the other end of the gate electrode 9 to be adjacent to one end of the
20 gate oxide film 7A. That is, a high concentration (N+ type) source region 10 is formed to be adjacent to one end of the gate electrode 9. Then, a high concentration (N+ type) drain region 11 is formed at a region separated from the other end of the gate electrode

9 (to be adjacent to the other end of the first gate oxide film
7A) in the second low concentration drain region 6. At this time,
arsenic ions are ion-implanted with an acceleration voltage of
about 80 KeV at a dose of about $6 \times 10^{15}/\text{cm}^2$.

5 Although description shown in the figure is omitted,
source-drain electrodes are formed through contact holes after
forming an insulation film between layers over whole surface
forming the contact holes on the insulation film between layers
to make contact with the source-contact regions.

10 Thus, in the method for manufacturing the semiconductor
device of the present invention, two kinds of impurities (phosphorus
and arsenic), which are ion-implanted previously on the surface
of the substrate and have different diffusion coefficients, are
treated thermally to induce diffusion. Using the difference in
15 the diffusion coefficients, a low concentration drain region
of a double structure having two kinds of impurity concentration
is formed. That is, the low concentration drain region is formed
to cover thinly the second low concentration (SLN type) drain
region 6 (based on arsenic ions) with the first low concentration
20 (LN type) drain region 5 (based on phosphorus ions). Therefore,
in contrast to changing impurity concentration uniformly over
the whole low concentration drain regions, the drain withstanding
voltage during operation can be improved independent of any

trade-off relationship of drain withstanding voltage at a low Vgs and drain withstanding voltage at a high Vgs.

According to the invention, by forming a low concentration drain region to have two kinds of different impurity concentrations, the low Vgs withstanding voltage withstands at the first low concentration drain region, and the high Vgs withstanding voltage withstands at the second low concentration drain region so as to improve the drain withstanding voltage characteristics during operation.

The first low concentration drain region and the second low concentration drain region are formed by thermally treating the two kinds of implanted impurities having different diffusion coefficients. Thus, the second low concentration drain can be formed in the first low concentration drain region so that the second low concentration drain is very close to the outer boundary of the first low concentration drain region.